

Serial No.:	10/605,100	Art Unit:	2818
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**IN THE ABSTRACT**

Please amend the abstract to read as follows:

-- In an SOI MOSFET device, with a silicon layer formed on a dielectric layer, a gate electrode stack is formed with sidewall spacers located ~~composed of sidewall spacer material on sidewalls thereof, of the gate electrode stack.~~ Raised source/drain regions are formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of gate polysilicon over a gate dielectric layer. The gate electrode stack is formed on the surface of the silicon layer. A cap layer in the top gate electrode surface is implanted with silicon or germanium. A plug of dielectric material which may comprise sidewall spacer material fills a notch on the edges of ~~[[a]]~~ the cap layer above the gate polysilicon and beneath a hard mask layer that overlies the cap layer. The sidewall spacers cover the sidewalls of the gate electrode ~~are covered by the sidewall spacers which cover and~~ a portion of the plug ~~for the purpose of eliminating the~~ to eliminate exposure of the gate polysilicon [,] to avoid formation of spurious epitaxial growth during the formation of raised source/drain regions. --

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